To: Dr. Tina Hudson
From: Julie Hasler and Tyra Correia
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Subject: ADC Project

The memo overviews the completion of a continuity, lower edge offset error, upper edge offset error, INL and DNL tests for two ADC0831 chips. For continuity, we input a current to each pin and measured the voltage across the pin, looking for a diode voltage drop that would indicate functional ESD protection circuitry and show that the chip has no shorts. For future calculations, the conversion from volts to LSBs was calculated using the standard testing voltage of 5.0V and the 256 possible codes from this 8-bit ADC.

$$V_{lsb} = \frac{5\ V}{2^8} = 19.53125\ mV$$

For the lower edge offset error, we started the input voltage at -0.005V and swept this voltage in increments of 0.1mV until either the measured digital output became code 1, or the input voltage became 40mV. The final input voltage was then converted to LSBs and compared to the ideal location for the lower edge,1 LSB, as seen in the following equation. This zero-scale error was datalogged to the datasheet specification of ±1 LSB.

$$EZS = \frac{V_{in}[LE]}{V_{lsb}} - 1$$

For the upper edge offset error, we started the input voltage at 4.958V and swept this voltage in increments of 0.1mV until either the measured digital output became code 255, or the input voltage became 5.02V. The final input voltage was then converted to LSBs and compared to the ideal location for the lower edge, 255 LSB as seen in the following equation. This full-scale error was datalogged to the datasheet specification of ±1 LSB.

$$EFS = \frac{V_{in}[UE]}{V_{lsb}} - 254$$

Finally, we were able to sweep the full range and develop a histogram spanning 256 bins using three different resolutions. Havg was calculated using the number of "hits" for all codes except for the 0 and full-scale codes. The codewidth and DNL was calculated using the number of hits normalized by Havg. Then INL for each code was calculated using the sum of the DNL from all previous codes, shown in the following three equations.

$$Havg = \sum_{i=1}^{254} Hist[i]$$

$$DNL[i] = codewidth[i] - 1 = \frac{Hist[i]}{Havg} - 1$$

$$INL[i] = \sum_{k=1}^{i} DNL[k]$$

We struggled with capturing the data output from the ADC. Somehow, our vector editor for the linearity tests stopped working between weeks and we could not figure out what went wrong. Eventually, we made a new one with the same parameters and it worked immediately. Another challenge was converting the data from INT64 data structures to int, but Dr. Hudson's guidance became very useful. Finally, doing the histogram test with 3 different resolutions forced us to make that code more modular.

The continuity test was very repeatable for both chips as the amount of variation for each pin on each chip was less than 2mV. We do see fabrication variation between the chips as they do not have any of the same values for continuity. We validated this data based on the datalogged results being approximately one diode drop. The zero-scale error test was not particularly repeatable. It passed every test, but it had a variation greater than 0.3 LSB for chip 2. The full-scale error test had less variation (around 0.1 LSB) which is not great, but it can be solved with guardbanding. These two tests were validated by stepping through their sweeps and paying attention to the data within the INT64 and our converted data.

For the histogram test, we looked at three different resolutions as seen in Table 2, Table 3, and Table 4. We validated our code by looking at the histogram as it was being filled, then copying this data to develop the visual histogram in Appendix C. We could see that the chip would pass DNL and INL specifications because the lowest number of hits was 16 and the highest number was 25 hits, corresponding to -20% and +25% from where they should have been. DNL seems to generally be repeatable at a resolution of Vlsb/10 as it does not vary more than 0.001 LSB. It is also worth noting that it generally remains the same size, so the maximum DNL likely comes from the same step. INL has more variation between tests which is concerning, but a measurement around 0.25 LSB gives enough room to guardband which chips pass. When the resolution is improved to Vlsb/20, the repeatability of DNL happens to look worse, but if test 5 is ignored, the variation looks the same. Due to the way DNL is calculated with a resolution of 20, possible values of DNL differ by 0.05 LSB, rather than 0.1LSB from a Vlsb/10 resolution. If the actual DNL is 0.276 LSB, then it would usually round to 0.3LSB, but with noise, it could round to 0.25 LSB. The increased resolution would reduce the amount of guardbanding needed. Worsening the resolution to Vlsb/5 showed a repeatable DNL, although this measurement would require a significant amount of guardbanding. The repeatability for INL looks bad because the only possibilities for values are 0, 0.2, 0.4, 0.6, 0.8, and 1.0 LSB.

In terms of timing, using a resolution of Vlsb/20 took over 3 seconds to complete, which is an expensive amount of time for a single test. Worsening the resolution to Vlsb/10 reduces the test time by approximately one-half, which is still 1.5 seconds. Depending on the fabrication variation of the part and how much large guardbands affect yield, it makes sense to a resolution closer to Vlsb/5 to have a smaller test time.

Table 1: DNL, INL, Continuity, Zero- Scale, and Full-Scale Data for chip 1 with resolution of ~2mV

Test	1	2	3	4	5	Lower Limit	Upper Limit	Units
ContVminus	-0.732	-0.732	-0.732	-0.732	-0.732	-1.0	-0.5	V
ContVref	-0.630	-0.630	-0.630	-0.630	-0.630	-1.0	-0.5	V
ContSclk	-0.732	-0.732	-0.732	-0.731	-0.731	-1.0	-0.5	V
ContSdata	-0.671	-0.671	-0.671	-0.670	-0.670	-1.0	-0.5	V
Cont/CS	-0.605	-0.605	-0.605	-0.604	-0.604	-1.0	-0.5	V
ContVplus	-0.732	-0.732	-0.732	-0.732	-0.732	-1.0	-0.5	V
ContVdd	-0.732	-0.732	-0.732	-0.732	-0.732	-1.0	-0.5	V
EZS	-0.652	-0.616	-0.636	-0.805	-0.662	-1.0	1.0	LSB
EFS	-0.592	-0.592	-0.623	-0.633	-0.521	-1.0	1.0	LSB
DNL	-0.300	-0.300	-0.300	-0.301	-0.301	-1.0	1.0	LSB
INL	0.218	0.222	0.219	0.243	0.324	-1.0	1.0	LSB

Table 2: DNL, INL, Continuity, Zero- Scale, and Full-Scale Data for chip 2 with resolution of ~2mV

Test	1	2	3	4	5	Lower Limit	Upper Limit	Units
ContVminus	-0.737	-0.737	-0.737	-0.737	-0.737	-1.0	-0.5	V
ContVref	-0.634	-0.634	-0.634	-0.634	-0.634	-1.0	-0.5	V
ContSclk	-0.736	-0.736	-0.736	-0.736	-0.736	-1.0	-0.5	V
ContSdata	-0.679	-0.679	-0.679	-0.679	-0.679	-1.0	-0.5	V
Cont/CS	-0.609	-0.609	-0.609	-0.609	-0.608	-1.0	-0.5	V
ContVplus	-0.737	-0.737	-0.737	-0.737	-0.737	-1.0	-0.5	V
ContVdd	-0.737	-0.737	-0.737	-0.737	-0.737	-1.0	-0.5	V
EZS	-0.560	-0.667	-0.908	-0.601	-0.770	-1.0	1.0	LSB
EFS	-0.613	-0.654	-0.592	-0.649	-0.603	-1.0	1.0	LSB
DNL	0.300	0.301	0.300	0.300	0.301	-1.0	1.0	LSB
INL	0.200	0.263	0.200	0.200	0.249	-1.0	1.0	LSB

Table 3: DNL, INL, Continuity, Zero- Scale, and Full-Scale Data for chip 2 with resolution of ~1mV

Test	1	2	3	4	5	Lower Limit	Upper Limit	Units
ContVminus	-0.737	-0.737	-0.737	-0.737	-0.737	-1.0	-0.5	V
ContVref	-0.634	-0.635	-0.634	-0.634	-0.634	-1.0	-0.5	V
ContSclk	-0.736	-0.736	-0.736	-0.736	-0.736	-1.0	-0.5	V
ContSdata	-0.679	-0.679	-0.679	-0.679	-0.679	-1.0	-0.5	V
Cont/CS	-0.679	-0.609	-0.609	-0.609	-0.609	-1.0	-0.5	V
ContVplus	-0.737	-0.737	-0.737	-0.737	-0.737	-1.0	-0.5	V
ContVdd	-0.737	-0.737	-0.737	-0.737	-0.737	-1.0	-0.5	V
EZS	-0.601	-0.621	-0.565	-0.585	-0.621	-1.0	1.0	LSB
EFS	-0.644	-0.592	-0.592	-0.659	-0.633	-1.0	1.0	LSB
DNL	0.250	0.250	0.250	0.250	0.300	-1.0	1.0	LSB
INL	-0.187	-0.187	-0.189	-0.187	-0.242	-1.0	1.0	LSB

Table 4: DNL, INL, Continuity, Zero-Scale, and Full-Scale Data for chip 2 with resolution of ~4mV

Test	1	2	3	4	5	Lower Limit	Upper Limit	Units
ContVminus	-0.737	-0.737	-0.737	-0.737	-0.737	-1.0	-0.5	V
ContVref	-0.634	-0.634	-0.634	-0.634	-0.634	-1.0	-0.5	V
ContSclk	-0.736	-0.736	-0.736	-0.735	-0.736	-1.0	-0.5	V
ContSdata	-0.679	-0.679	-0.679	-0.679	-0.679	-1.0	-0.5	V
Cont/CS	-0.609	-0.609	-0.609	-0.609	-0.608	-1.0	-0.5	V
ContVplus	-0.737	-0.737	-0.737	-0.737	-0.737	-1.0	-0.5	V
ContVdd	-0.737	-0.737	-0.737	-0.737	-0.737	-1.0	-0.5	V
EZS	-0.596	-0.590	-0.626	-0.611	-0.560	-1.0	1.0	LSB
EFS	-0.577	-0.597	-0.633	-0.700	-0.613	-1.0	1.0	LSB
DNL	-0.400	-0.400	-0.400	-0.400	0.400	-1.0	1.0	LSB
INL	-0.200	-0.400	-0.200	-0.200	-0.200	-1.0	1.0	LSB

We were able to perform five tests on the first chip at a resolution of Vlsb/10 to get an average of 10 hits per code which may be found in Table 1. According to the results, the continuity data was highly repeatable across the five tests. The offset error demonstrated the least amount of repeatability and deviated by 0.189V. In comparison the gain error deviated by 0.112V and the INL deviated by 0.106LSB. The DNL results proved highly repeatable and remained consistent at -0.3LSB across all five tests.

We then performed five tests on the second chip at a resolution of Vlsb/10 to get 10 hits per code, which may be found in Table 2. Upon closer examination, all pins except for /CS demonstrated reproducible results and deviated less than 0.01V across both chips. The /CS demonstrated the most deviation at 0.132V across both chips. Additionally, the offset error in chip 2 at a 2mV resolution deviated by 0.348V which was higher in comparison to chip 1. The gain error deviated by 0.062V and INL deviated by 0.063LSB. These results on the other hand depict a better performance for repeatability in chip 2. The DNL demonstrated roughly the same performance and also remained highly repeatable at +0.3LSB. Furthermore, the continuity results for all pins were highly repeatable and did not deviate in the slightest across all five tests.

The resolution was then changed to Vlsb/20 for chip 2 to get 20 hits per code, and five tests were subsequently performed. The results of the tests may be found in Table 3. The high test repeatability of continuity measurements can still be observed at the higher resolution on chip 2. The increase in resolution portrays a distinct increase in repeatability across the offset error and INL which all decreased significantly. The offset error deviated by 0.056V, whereas the INL deviated by 0.055LSB. Surprisingly, the gain error performed slightly worse deviating by 0.067V compared to 0.063V at a 2mV resolution. Similarly, the DNL results also performed worse a deviation of 0.05V compared to the 0.001LSB at a 2mV resolution.

The resolution was then decreased to Vlsb/5 for chip 2 to get 5 hits per code on average, and five tests were subsequently performed. Because we expect 5 hits for each code, the possible passing values for INL and DNL are approximately 0, 0.2, 0.4, 0.6, 0.8, and 1.0, so if every test happens to get close to the same value, it will look very repeatable. As seen in Table 4, this is what happened to DNL. However, for INL, one of the tests had a different result and the low resolution makes it look like an outlier. Offset voltage and full-scale error have been as repeatable as they had been previously.